CLAIMS

1. A device comprising an array of pixels, each pixel including a pixel element (16) and being associated with a switching circuit (60), wherein the switching circuit (60) is for selectively routing one of at least two inputs (Vdrive1, Vdrive2; Vdrive1, 12) to the pixel element (16), comprising at least first and second switching transistors (50; 14,50) connected between a respective one of the at least two inputs and the pixel element, wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs, and wherein a capacitive connection (C_B) is provided between the gate of at least one of the switching transistors and an output of the switching transistor.

2. A device as claimed in claim 1, wherein the data signal for each switching transistor is routed to the gate of the switching transistor by a transfer switch (42) which controls the timing of application of the data signal for each switching transistor (50), and wherein a capacitive connection (C_B) is provided between the gate of each switching transistor (50) and the output (62) of each switching transistor.

3. A device as claimed in claim 2, wherein a capacitive connection (C_B) is provided between the gate of each switching transistor (50) and an output (62) of the switching circuit.

4. A device as claimed in any preceding claim, wherein the gates of the first and second switching transistors (50) are connected together and the capacitive connection comprises a capacitor connected between the gates and an output (62) of the switching circuit.

5. A device as claimed in claim 4, wherein the first switching transistor (50) is an n-type transistor and the second switching transistor (50) is a p-type transistor.

6. A device as claimed in any one of claims 1 to 3, wherein the capacitive connection comprises a respective capacitor connected between the gate of each switching transistor and an output (62) of the switching circuit.

7. A device as claimed in claim 6, comprising n inputs, where n is greater than 2, and comprising first to nth switching transistors (50) connected between a respective one of the n inputs (signal1-signal4) and the pixel element, and wherein the data signals for each switching transistor are selected such that an individual one of the switching transistors is turned on to route the respective input to the pixel element (16).

8. A device as claimed in claim 7, wherein at least one of the switching transistors is n-type and at least one of the switching transistors in p-type.

9. A device as claimed in claim 7, wherein all switching transistors are of the same polarity type.

10. A device as claimed in claim 6, comprising n inputs, and comprising first to nth switching transistors (50a-50d) connected between a respective one of the n inputs (signal0-signal3) and one of two intermediate outputs (56,58), and wherein the data signals for each switching transistor are selected such that half of the switching transistors are turned on to route a first selected input to one intermediate output (56) and to route a second selected input to the other intermediate output (58).

11. A device as claimed in claim 10, further comprising a switching circuit (54) for selectively routing one of the intermediate outputs (56,58) to the pixel element.

12. A device as claimed in any one of claims 1 to 5 comprising an active matrix liquid crystal display device in which the pixel elements comprise liquid crystal cells, each pixel comprising the switching circuit (60) for routing one of two voltage drive levels (Vdrive1,Vdrive2) to the pixel element (16).

13. A device as claimed in claim 12, further comprising:

a first selection switch (64) between the common output (62) of the switching circuit (60) and the liquid crystal cell of the pixel (16); and

a second selection switch (14) between an analogue pixel data line (12) and the liquid crystal cell (16) of the pixel.

14. A device as claimed in claim 13, wherein the two voltage drive levels comprise voltages for driving the liquid crystal cell to a black and a white state.

15. A device as claimed in claim 13 or 14, wherein the control signal for selecting which one of the two voltage drive levels is to be routed to the pixel element is provided on the analogue pixel data line (12).

16. A device as claimed in claim 15, wherein the data signal for each switching transistor (50) is routed to the gate of the switching transistor by a transfer switch (42) which controls the timing of application of the data signal for each switching transistor (50), and wherein a capacitive connection (C_B) is provided between the gate of each switching transistor (50) and the output (62) of each switching transistor, and wherein the transfer switch (42) is provided between the analogue pixel data line (12) and the gates of the first and second switching transistors (50).

17. A device as claimed in claim 12, further comprising:

a first selection switch (64) between the output of the at least one of the switching transistors (50) and the liquid crystal cell of the pixel; and

a second selection switch (14) between an analogue pixel data line (12) and the liquid crystal cell of the pixel.

18. A device as claimed in claim 17, wherein the second selection switch (14) comprises the other of the first and second switching transistors.

19. A device as claimed in claim 18, wherein in a first mode, the second selection switch (14) provides one of two digital pixel signals from the analogue pixel data line (12) to the liquid crystal cell (16), and in a second mode the second selection switch (14) provides an analogue pixel signal from the analogue pixel data line (12) to the liquid crystal cell (16).

20. A method of routing one of at least two inputs to a pixel element within a pixel of a device comprising an array of pixels, the method comprising:

applying data signals to the gates of at least first and second switching transistors (50) connected between a respective one of the at least two inputs (signal1-signal4) and the pixel element (16) to turn on a selected one of the first and second switching transistors (50) and turn off the other of the first and second switching transistor (50), thereby routing the respective input to the pixel element (16),

wherein the timing of application of the data signals is selected in dependence on the signals on at least one of the two inputs,

wherein a capacitive connection (C_B) is provided between the gate of at least one switching transistor (50) and an output of the switching transistor, and

wherein the timing is controlled such that the capacitive connection reduces the required voltage swing in the data signal between that required to turn on and turn off a switching transistor.

21. A method of driving a liquid crystal display, comprising:

in a first mode, switching analogue pixel drive signals to each pixel of the display; and

in a second mode, routing one of two pixel drive signals on respective inputs to each pixel of the display, the routing for each pixel in the second mode using the method of claim 20.

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